respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

WHAT IS CLAIMED IS:

1. A method of processing a semiconductor device comprising the steps of:

applying photo-resist to the surface of a substrate to be processed;

rendering exposure of a first overlay measurement mark and a first pattern to the substrate coated with the photo-resist by using a first exposure tool which is fitted up with a first mask;

processing the substrate, which has been rendered the exposure of the first pattern, to form thereon a first overlay measurement mark and a first circuit pattern;

applying photo-resist to the substrate surface on which the first overlay measurement mark and first circuit pattern have been formed;

rendering the exposure of a second overlay measurement mark and a second pattern to the substrate coated with the photo-resist by using a second exposure tool which is fitted up with a second mask;

processing the substrate, which has been rendered the exposure of the second overlay measurement mark and second pattern, to form thereon a second overlay measurement mark and a second circuit pattern; and

wherein said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask

modifies the exposure condition of the second overlay measurement mark and second pattern by using information on the exposure distortion caused by the first exposure tool and information on the exposure distortion caused by the second exposure tool.

2. A method of processing a semiconductor device according to claim 1, wherein said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask further uses information resulting from the measurement of the overlay accuracy between the first overlay measurement mark and second overlay measurement mark which is derived from the measurement of the substrate, which has been rendered the exposure of the second overlay measurement mark and second pattern over the first overlay measurement mark formed in advance, and the overlay accuracy between the first circuit pattern and second pattern in modifying the exposure condition of the second overlay measurement mark and second pattern.

3. A method of processing a semiconductor device according to claim 1, wherein said exposure condition of second pattern to be modified in said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask includes any of the positional shift, rotation and magnification factor of the second pattern resulting from the

rendition of exposure on the surface of the substrate.

4. A method for processing a semiconductor device according to claim 1, wherein said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask further uses information on the disparity between the first mask and second mask indicated by the exposure distortion of the first overlay measurement mark and the exposure distortion of the second overlay measurement mark and information on the disparity between the first mask and the second mask indicated by the exposure distortion of the first pattern and the exposure distortion of the second pattern, in modifying the exposure condition of the second overlay measurement mark and second pattern.

5. A method of processing a semiconductor device according to claim 1, wherein said information on the exposure distortion caused by the first exposure tool and information on the exposure distortion caused by the second exposure tool used in said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask are stored in a memory in advance.

6. A method for processing a semiconductor device according to claim 1 further including the step of displaying information on the overlay accuracy between the first circuit pattern and the second circuit pattern.

7. A method of processing a semiconductor device comprising the steps of:

applying photo-resist to the surface of a substrate to be processed;

rendering exposure of a first overlay measurement mark and a first pattern to the substrate coated with the photo-resist by using a first exposure tool which is fitted up with a first mask;

processing the substrate, which has been rendered the exposure of the first pattern, to form thereon a first overlay measurement mark and a first circuit pattern;

applying photo-resist to the substrate surface on which the first overlay measurement mark and first circuit pattern have been formed;

rendering the exposure of a second overlay measurement mark and a second pattern to the substrate coated with the photo-resist by using a second exposure tool which is fitted up with a second mask;

processing the substrate, which has been rendered the exposure of the second overlay measurement mark and second pattern, to form thereon a second overlay measurement mark and a second circuit pattern; and

wherein said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask modifies the exposure condition of the second overlay

measurement mark and second pattern by using information resulting from the measurement of the overlay accuracy between the first overlay measurement mark and second overlay measurement mark which is derived from the measurement of the substrate, which has been rendered the exposure of the second overlay measurement mark and second pattern over the first overlay measurement mark formed in advance, information on the disparity between the first mask and second mask indicated by the exposure distortion of the first overlay measurement mark and the exposure distortion of the second overlay measurement mark, and information on the disparity between the first mask and second mask indicated by the exposure distortion of the first pattern and the exposure distortion of the second pattern.

8. A method for processing a semiconductor device according to claim 7, wherein said exposure condition of second pattern to be modified in said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask includes any of the positional shift, rotation and magnification factor of the second pattern resulting from the rendition of exposure on the surface of the substrate.

9. A method for processing a semiconductor device according to claim 7, wherein said information on the exposure distortion caused by the first exposure tool and information on the exposure distortion caused by the second exposure tool

used in said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask are stored in a memory in advance.

10. A method for processing a semiconductor device according to claim 7, further including the step of displaying information on the overlay accuracy between the first circuit pattern and the second circuit pattern.

11. A method for processing a semiconductor device comprising the steps of:

applying photo-resist to the surface of a substrate to be processed;

rendering exposure of a first overlay measurement mark and a first pattern to the substrate coated with the photo-resist by using a first exposure tool which is fitted up with a first mask;

processing the substrate, which has been rendered the exposure of the first overlay measurement mark and first pattern, to form thereon a first overlay measurement mark and a first circuit pattern;

applying photo-resist to the substrate surface on which the first overlay measurement mark and first circuit pattern have been formed;

rendering the exposure of a second overlay measurement mark and a second pattern to the substrate coated with the photo-resist by using a second exposure tool which is fitted

up with a second mask;

processing the substrate, which has been rendered the exposure of the second pattern inclusive of the second overlay measurement mark, to form thereon a second overlay measurement mark and a second circuit pattern; and

wherein said step of rendering the exposure of the second pattern by using the second exposure tool fitted up with the second mask modifies the exposure condition of the second pattern by use of the second exposure tool fitted up with the second mask by using information on the exposure distortion of the first pattern which has been formed by using the first exposure tool fitted up with the first mask and information on the exposure distortion of the second pattern which has been formed by using the second exposure tool fitted up with the second mask.

12. A method for processing a semiconductor device according to claim 11, wherein said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask further uses information resulting from the measurement of overlay which is derived from the measurement of the substrate, which has been rendered the exposure of the second overlay measurement mark and second pattern over the first overlay measurement mark formed in advance, in modifying the exposure condition of the second overlay measurement mark and second pattern.

13. A method for processing a semiconductor device according to claim 11, wherein said information on the exposure distortion caused by the first exposure tool and information on the exposure distortion caused by the second exposure tool used in said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask are stored in a memory in advance.

14. A method for processing a semiconductor device according to claim 11, further including the step of displaying information on the overlay accuracy between the first circuit pattern and the second circuit pattern.

15. A method for processing a semiconductor device comprising the steps of:

applying photo-resist to the surface of a substrate to be processed;

rendering the exposure of a first overlay measurement mark and a first pattern to the substrate coated with the photo-resist by using a first exposure tool which is fitted up with a first mask;

processing the substrate, which has been rendered the exposure of the first overlay measurement mark and first pattern, to form thereon a first overlay measurement mark and a first circuit pattern;

applying photo-resist to the substrate surface on which the first overlay measurement mark and first circuit

pattern have been formed;

adjusting the exposure condition of the second exposure tool which is fitted up with the second mask by using information resulting from the measurement of overlay which is derived from the measurement of the substrate which has been rendered the exposure of the second overlay measurement mark and second pattern over the first overlay measurement mark and first pattern formed in advance and information on the exposure distortion caused by the first exposure tool and exposure distortion caused by the second exposure tool;

rendering the exposure of the second overlay measurement mark and second pattern to the substrate coated with the photo-resist by using the second exposure tool having its exposure condition adjusted and having the second mask; and

processing the substrate, which has been rendered the exposure of the second pattern inclusive of the second overlay measurement mark, to form thereon a second overlay measurement mark and a second circuit pattern.

16. A method for processing a semiconductor device according to claim 15, wherein said step of adjusting the exposure condition of the second exposure tool fitted up with the second mask further uses information on the disparity between the first mask and the second mask indicated by the exposure distortion of the first overlay measurement mark and the exposure distortion of the second overlay measurement mark

and information on the disparity between the first mask and the second mask indicated by the exposure distortion of the first pattern and the exposure distortion of the second pattern.

17. A system for processing a semiconductor device comprising:

a memory unit which stores exposure distortion data of the exposure field of a first and second exposure tools, and coordinate data of a device area and position data of an overlay measurement mark in the exposure field;

a modification value calculating unit which calculates the exposure distortions of the device area and the exposure distortions at the overlay measurement mark position caused by the first and second exposure tools from the exposure field distortion data of the exposure field of the first and second exposure tools stored in said memory unit based on the coordinate data of device area and position data of overlay measurement mark in the exposure field stored in the memory unit, calculates the difference between the calculated exposure distortions of device area of the first and second exposure tools and the difference between the calculated exposure distortions at overlay measurement mark position of the first and second exposure tools, and calculates a modification value which relates both differences to each other;

an overlay measuring tool which measures the overlay

of the exposure field by the second exposure tool based on the measurement of a subject of exposure which has been rendered in the past by being registered with reference to the overlay measurement mark by the second exposure tool;

a first exposure condition correction value calculating unit which calculates a first exposure condition correction value for a reference exposure field of the second exposure tool based on the measurement result of overlay of the exposure field of the second exposure tool provided by said overlay measuring tool;

a second exposure condition correction value calculating unit which calculates a second exposure condition correction value for the device area of the second exposure tool by modifying the first exposure condition correction value calculated by said first exposure condition correction value calculating unit with a modification value which is calculated in the process of calculation of the modification value; and

wherein the second exposure condition correction value calculated by said second exposure condition correction value calculating unit is fed back to the second exposure tool, based on which feedback the second exposure tool carries up the overlap exposure.

18. A system for processing a semiconductor device according to claim 17, further including judging unit which calculates an assessment value of the overlay of device area

by modifying the result of measurement of overlay of the exposure field provided by said overlay measuring tool with the modification value calculated by said modification value calculating unit, and compares the calculated overlay assessment value with a criterion value of overlay between a first and second layers thereby to judge the approval of overlay accuracy of the second layer with respect to the first layer in the device area.

19. A system for processing a semiconductor device according to claim 17, further including output unit which releases the result of judgment made by said judging unit of the approval of overlay accuracy of the second layer with respect to the first layer in the device area.

20. A system for processing a semiconductor device according to claim 17, wherein said modification value calculating unit comprises a host computer which connects the first and second exposure tools through a network.